TECHNICAL INFORMATION
FOR TEKTRONIX CUSTOMERS

VOLUME 12 NUMBER 4
DECEMBER 1980

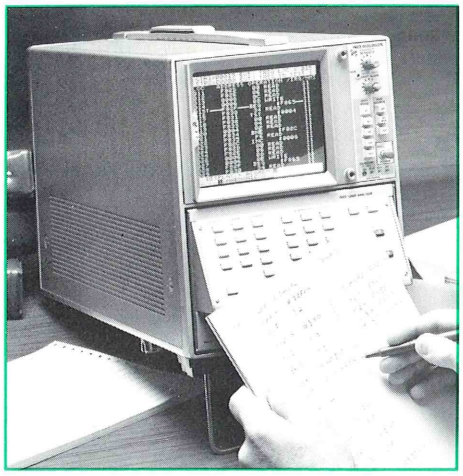
Tekscope

Tektronix®
COMMITTED TO EXCELLENCE

Tekscope CONTENTS

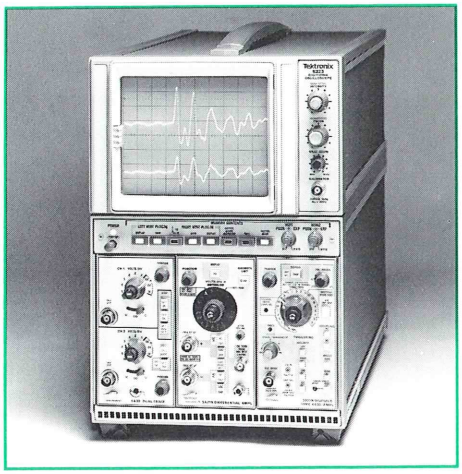
A User-Programmable Logic Analyzer for Microprocessor Design

The new Tektronix 7D02 Logic Analyzer is primarily a tool for designing, debugging, and troubleshooting microprocessor systems. It can support 8-bit and 16-bit microprocessors. The 7D02 can acquire up to 28 channels (44 optionally) of synchronous data. A timing option adds an additional eight channels of synchronous data or eight channels of asynchronous timing or state information.



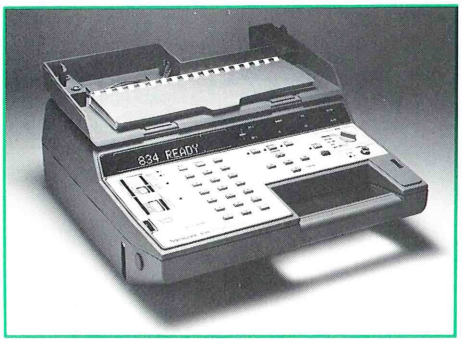
Digital Storage and Plug-in Versatility Distinguish New 10-MHz 5000-Series Oscilloscope

The new 5223 Digitizer Oscilloscope offers some exciting new capabilities for making measurements in the areas of mechanical design, such as structural and engine performance testing; biomedical research, such as stimulus response and EMG studies; and similar types of applications.



A Programmable Data Communications Tester for First-Line Technicians

The 834 Data Communications Tester provides both monitoring and simulation of data terminal equipment and data communications equipment, such as modems. User-insertable ROM Packs provide extended programming capabilities and allow customers to design tests specifically for their systems. Highly portable, inexpensive, and easy to operate, the 834 is intended primarily for use by the first-line technician.



New Products

A host of new products, including a new microprocessor-development-laboratory family, a sophisticated semiconductor test system, high-resolution hard copy unit, and others are presented in this issue.

Tektronix, Inc. is an equal opportunity employer.

Customer information from Tektronix, Inc.
Beaverton, Oregon 97077

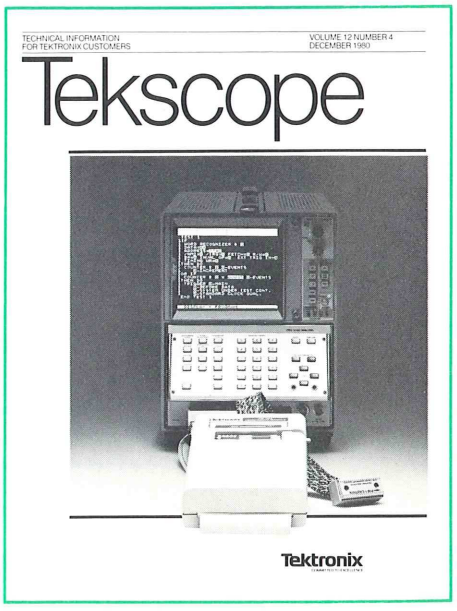
Tekscope is a quarterly publication of Tektronix, Inc. In it you will find articles covering the entire scope of Tektronix' products. Technical articles discuss what's new in circuit and component design, measurement capability, and measurement technique.

Editor: Gordon Allison
Graphic Designer: Michael Satterwhite

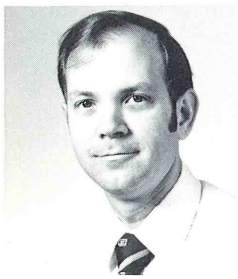
Cover:

The 7D02 Logic Analyzer can be readily configured for a particular microprocessor by simply plugging in the appropriate personality module. The 6802 Personality Module is in use in this instance.

Cover photo by Steven Fish.



A User-Programmable Logic Analyzer for Microprocessor-Based Design



Mike Reiney, project manager for the 7D02, joined Tek in 1971 following receipt of his Bachelor's and Master's degrees in electrical engineering from Rice University. Mike was involved in the design of several TM 500 Series products before joining the Logic Analyzer design group. In his spare time Mike enjoys skiing, sailing, and motorcycling.

The logic analyzer is the basic tool for designing and debugging digital circuitry. The characteristics of a logic analyzer designed for working with random-logic systems differ considerably from those required for working with microprocessor-based systems. Random-logic analyzers usually emphasize sampling speed and depth of memory, while analyzers suitable for working with microprocessor systems feature a large number of input channels and extremely flexible triggering.

The new Tektronix 7D02 Logic Analyzer is primarily a tool for designing, debugging, and troubleshooting microprocessor systems. It can support both 8-bit and 16-bit microprocessors.

The 7D02 can acquire up to 28 channels (44 optionally) of synchronous data, and an additional eight channels of synchronous data or eight channels of asynchronous timing or state information are available through a timing option, for a total of 52 channels. With the timing option installed, the 7D02 is one of the most powerful, yet easy to use, tools available for working with microprocessor systems.

The 7D02 can be easily programmed (through a front-page keypad) to follow the complex sequences of events occurring in the system under test. Program displays are dynamic and interactive, with only necessary prompting on-screen at any given time.

As the programming cursor is moved, new prompting occurs. Menus default to reasonable values to simplify input, and the 7D02 assumes the most logical program and supplies intermediate program steps. Displayed data can be formatted in the basic radices and mnemonics pertinent to the microprocessor under test.

A series of personality modules adapt the 7D02 to the clock and bus characteristics of individual microprocessors. The basic 7D02 contains four word recognizers, two general-purpose counters, a user-configurable clock, data-qualification circuitry, programmable state machine, and three memories.

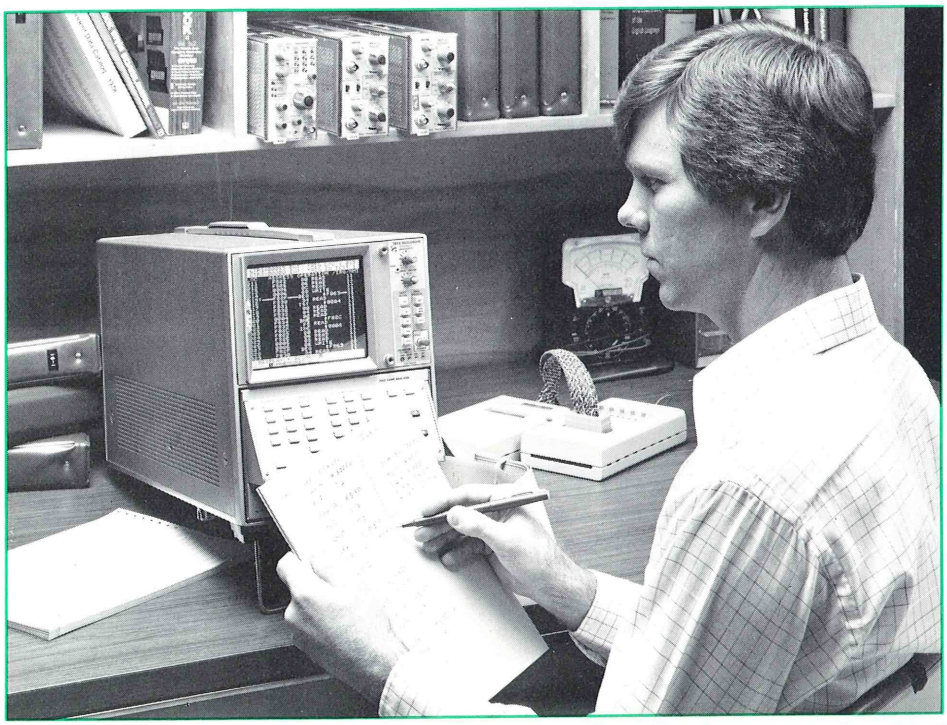


Fig. 1. The 7D02 Logic Analyzer is a versatile user-programmable tool for microprocessor-based design.

A programmable state machine

The programmable state machine is the key to the 7D02's flexibility. It provides two equally powerful capabilities — generation of a trigger algorithm that tracks the complex, convoluted program flow to trigger exactly where the user requires, and data qualification that determines precisely which data will be stored in the acquisition memory. In the 7D02, the qualify command works exactly like the trigger command. The user can employ these two commands to discard the bus transactions of no consequence and to store only that data which is of interest in solving the problem.

The user can program the 7D02's state machine for any one of four states, with each state representing a user-determined output that is the result of a user-determined input. The state-machine input consists of lines from the four word recognizers and two counters; the output consists of individual lines to the main trigger, timing option trigger, data qualifier, and four lines to control the two counters.

The inputs from the word recognizers and counters are called ***events,*** and the outputs are called ***commands.*** When programming the 7D02, the user can link any event or combination of events to any command or combination of commands. The state machine executes in real time with the system-under-test and can enter any of its states in any order, any number of times. These capabilities allow the user to program the 7D02 to follow the complex sequences encountered in microprocessor-based systems.

Block-structured programming language

The 7D02 programs with a block-structured language. The programming language uses four tests, each constructed using an IF-THEN-ELSE syntax. This syntax makes the execution of a command conditional on the occurrence of an event. Events are keyed in following an IF or an OR IF prompt, and commands are keyed in following a THEN DO or ELSE DO prompt. The user can have as many OR IF — THEN DO clause pairs as necessary (subject to memory limitations), but there can be only one ELSE clause in each test.

Only one test may be active at a time. The user moves from one test to another by executing a GO TO command. The following example shows a program containing two tests and illustrates moving from one test to another. This operation represents a two-level sequential trigger.

```
 TEST 1
1 IF
1  WORD RECOGNIZER #1
1  DATA = XX
1  ADDRESS = 4325
1  /NMI = X    /IRQ = X    FETCH = X    R/W = X
1  BA = X    INVAL OP = X    EXT TRIG IN = X
1  TIMING WR = X
1 THEN DO
1  GOTO 2
  END TEST1
  TEST 2
2 IF
2  WORD RECOGNIZER #2
2  DATA = XX
2  ADDRESS = 694F
2  /NMI = X    IRQ = X    FETCH = X    R/W = X
2  BA = X    INVAL OP = X    EXT TRIG IN = X
2  TIMING WR = X
2 THEN DO
2  TRIGGER 0-MAIN
2      0-BEFORE DATA
2      0-SYSTEM UNDER TEST CONT.
2      0-STANDARD CLOCK QUAL.
  END TEST 2
```

Pressing the 7D02 START button initiates TEST 1. When address 4325 is detected, the event in TEST 1 becomes TRUE and the GO TO (to TEST 2) is executed, deactivating TEST 1 and activating TEST 2. If address 694F is detected, the main acquisition memory will be triggered and data will be stored. Note that if address 4325 occurs again it will be ignored because TEST 1 is inactive. Entering this program required only three keystrokes plus filling in the field values.

Solving a practical problem

Now, let's consider a practical problem. Assume there is a location, OUTBUF, that is the character buffer for a computer line-printer. This location is only written-to from subroutine OUTCHAR. Unfortunately, data on the printer is not always what we expect. The problem is to determine whether location OUTBUF is being written-to from some other section of the code.

With a traditional logic analyzer, we could trigger on OUTBUF and examine the data result to see if the access was legitimate. We may have to examine many legitimate accesses before finding the problem access.

Using the 7D02 we can locate the illegitimate access quickly and easily. The program is shown in figure 2. The two events in TEST 1 are the detection of the addresses for OUTBUF and OUTCHAR. All events in a test are evaluated simultaneously. If the location OUTBUF is written to, the 7D02 will trigger. If the beginning of a subroutine OUTCHAR is detected, the 7D02 will progress to TEST 2. As there is no trigger in TEST 2, the 7D02 cannot trigger during TEST 2. When the end of subroutine OUTCHAR occurs, TEST 2 ends, and the 7D02 goes back to TEST 1. Thus, we see that the 7D02 will trigger and display data only when location OUTBUF is written to, and only if subroutine OUTCHAR is not running.

Now, let's assume that OUTBUF was never written-to from an improper location. If the error occurs at least once every several minutes (a reasonable time to wait for a trigger), the qualify command can be used to verify the accuracy of the data being written to OUTBUF. Figure 3 shows the addition to the program required to instruct the 7D02 to acquire only data written to OUTBUF. If the printer malfunctions, the user can manually stop this program. The contents of the trace memory can then be compared to the printed text by putting the 7D02 in the ASCII format mode.

If the error occurs very infrequently, or if the result of the previous exercise shows that correct data was being written to OUTBUF, we must employ a less direct means to solve the problem.

The two counters in the 7D02 can be used either to count discrete occurrences, or as timers. We can employ the counters to insert a fixed time period as a part of the

```
    TEST 1
1   IF
1    WORD RECOGNIZER # 1
1    DATA=XX
1    ADDRESS=051B
1    IO/M=X   INRQ=X   FETCH=X   R/W=0
1    INACK=X   HOLD=X   EXT TRIG   IN=X
1    TIMING WR=X
1   THEN DO
1    TRIGGER 0-MAIN
1       0-BEFORE DATA
1       0-SYSTEM UNDER TEST CONT
1       0-STANDARD CLOCK QUAL
1   OR IF
1    WORD RECOGNIZER # 2
1    DATA=XX
1    ADDRESS=9721
1    IO/M=X   INRQ=X   FETCH=1   R/W=X
1    INACK=X   HOLD=X   EXT TRIG IN=X
1    TIMING WR=X
1   THEN DO
1    GO TO 2
    END TEST 1
    TEST 2
2   IF
2    WORD RECOGNIZER # 3
2    DATA=C9
2    ADDRESS=XXXX
2    IO/M=X   INRQ=X   FETCH=1   R/W=X
2    INACK=X   HOLD=X   EXT TRIG IN=X
2    TIMING WR=X
2   THEN DO
2    GO TO 1
    END TEST 2
```

Fig. 2. This 7D02 program will trigger when location OUTBUF is written to, unless subroutine OUTCHAR is running at the same time. The PM104 (8085) personality module is being used. Word recognizer 1 is TRUE when OUTBUF (015B) is written to. Word recognizer 2 is TRUE on the first instruction of OUTCHAR (9721). Word recognizer 3 is TRUE when a RET instruction is executed indicating the end of OUTCHAR. Entering this extensive program required only eight keystrokes plus filling in the field values.

trigger, a feature which can be very useful in some instances, as the following example shows.

Hypothesizing that there is a timing error in the printer, we set up an experiment to determine if the setup time specification on the print head is being met. We start a counter when the character is written to OUTBUF. If the print hammer is actuated within 10 milliseconds, the timing specification is being violated and the 7D02 will trigger. The 7D02 program is shown in figure 4.

```
    QUALIFY
Q    STORE ONLY ON
Q    WORD RECOGNIZER # 1
Q    DATA=XX
Q    ADDRESS=051B
Q    IO/M=XX   INRQ=X   FETCH=1   R/W=0
Q    INACK=X   HOLD=X   EXT TRIG IN=X
Q    TIMING WR=X
Q   END QUALIFY
```

Fig. 3. Program additions required to qualify any write to 051B.

In this example, the external trigger line is connected to the hammer-driver signal and is defined in word recognizer 2 as a TRUE. Word recognizer 1 detects the write to OUTBUF.

TEST 1 waits for the write to OUTBUF. When this happens, the counter is started and TEST 2 is activated. In TEST 2 there is a race. If the hammer driver is actuated first,

```
    TEST 1
1   IF
1    WORD RECOGNIZER # 1
1    DATA=XX
1    ADDRESS=051B
1    IO/M=X   INRQ=X   FETCH=X   R/W=0
1    INACK=X   HOLD=X   EXT TRIG IN=X
1    TIMING WR=X
1   THEN DO
1    COUNTER # 1 2 MS
1       2 RESET AND RUN
1    GO TO 2
    END TEST 1
    TEST 2
2   IF
2    WORD RECOGNIZER # 2
2    DATA=XX
2    ADDRESS=XXXX
2    IO/M=X   INRQ=X   FETCH=X   R/W=X
2    INACK=X   HOLD=X   EXT TRIG IN=1
2    TIMING WR=X
2   THEN DO
2    TRIGGER 0 MAIN
2    2 AFTER DATA
2    0 SYSTEM UNDER TEST CONT 1
2    0 STANDARD CLOCK QUAL
2   OR IF
2    COUNTER # 1=00010 2 MS
2   THEN DO
2    GO TO 1
    END TEST 2
```

Fig. 4. Program to check timing margins. If OUTBUF (051B) is written to and the hammer driver is actuated (as indicated by the TRUE and EXT TRIG IN) before COUNTER #2 reaches 10 milliseconds, we know the timing specification has been violated. This program can be set up using only seven keystrokes plus filling in the field values.

the 7D02 triggers. If the timer runs out, sufficient setup time has elapsed and TEST 1 is actuated again.

It is possible for the 7D02 to loop between TEST 1 and TEST 2 millions of times without triggering. The 7D02 will trigger only when the timing constraint has been violated.

The 7D02 also could be easily programmed to check that every write to OUTBUF is followed by only one actuation of the print hammer.

The timing option

The triggering capability of the 7D02 makes it an ideal tool for integrating the hardware and software in a microprocessor-based system. However, conditions often require us to analyze the random-logic circuits associated with the microprocessor. The timing option available for the 7D02 provides this capability. With the timing option installed, the 7D02 is essentially two logic analyzers in one — a 52-channel synchronous analyzer (with expansion option), or a 44-channel synchronous analyzer plus an 8-channel asynchronous logic analyzer.

The timing option uses the 8-channel P6451 Logic Probe to acquire data. The timing option has its own 255 x 8-bit acquisition memory, 255 x 8-bit glitch memory, 8-channel word recognizer (the external trigger input provides a ninth nonstored channel), and an internal clock. The sampling rate is programmable over a range of 20 nanoseconds to 5 milliseconds. A programmable 0 to 300 nanosecond filter is provided for the word recognizer output.

You can establish the trigger relationship of the main and timing option sections in any manner you choose. For example, either or both sections can be triggered or armed from either or both sections. This extreme trigger versatility is useful for debugging the interaction between a microprocessor and its peripheral hardware.

Some design considerations

A simplified block diagram of the 7D02 is shown in figure 5. The ability to completely program the triggering and qualification algorithms requires the decision blocks (such as word recognizers and the state machine) to be implemented in random-access-memory (RAM), which places considerable time constraints on the real-time acquisition system. At the maximum rate of 10 megahertz, the word-recognizer RAMs require almost a full clock cycle for storage. Likewise, the counter subsystem and state machine require another clock cycle. The 7D02 uses a pipeline decision process for delaying data flow to allow time for producing complex signals such as triggers and qualifiers. The pipeline consists of two sets of data latches and the 256 x 44-bit acquisition memory. Words are consecutively clocked into the pipeline latches by the state clock signal; the same clock edge writes data into the acquisition RAM. If the qualify signal from the state machine is TRUE, then the RAM address counter increments. Otherwise, the next state clock overwrites the same memory cell and the word is, effectively, not stored.

The state machine is RAM-based also. The state-machine latch stores the signals from the word recognizers, the state-feedback bits from the RAM, and the feedback bits from the two counters. The latched data (which represents events in the user language) addresses a location in RAM that contains the data appropriate for the next operation. The data outputs from the state machine are the logic analyzer control lines and represent the commands issued by the user language.

The dual-counter subsystem is implemented with direct-memory-access controller ICs to conserve space and power. Under state-machine control, the glitchless start/stop allows resolution to be increased using time-interval-averaging techniques. One counter may be used as the loop counter for the averaged measurement, which is accumulated in the second counter.

Designing plug-in personality modules — to allow the 7D02 to accommodate many different microprocessors without dismantling the instrument to change personalities — presented an interesting challenge. To achieve the necessary flexibility, a programmable clock synthesizer is used and appropriate firmware is included in the personality module.

The 7D02 clock synthesizer can shift or divide the input clock by up to four clock cycles or times to accommodate multiphase clocks. A programmable external synchronizer (Esync) locks the 7D02 to the system under test. A programmable wait-state generator tracks microprocessor wait states.

The programmable clock shifter is a universal shift register (see figure 6). It is loaded by the Esync signal. The wait signal asserts the hold line to suspend shifting. The clock divider adds feedback around the shifter. The Esync and wait signals are generated from the information provided by the hardware and by the firmware in the personality module.

The personality module

The personality module contains input buffers, bus demultiplexers, special control generators, and firmware. The personality module firmware provides information to program the 7D02 clock synthesizer and clock qualifier. It also provides information

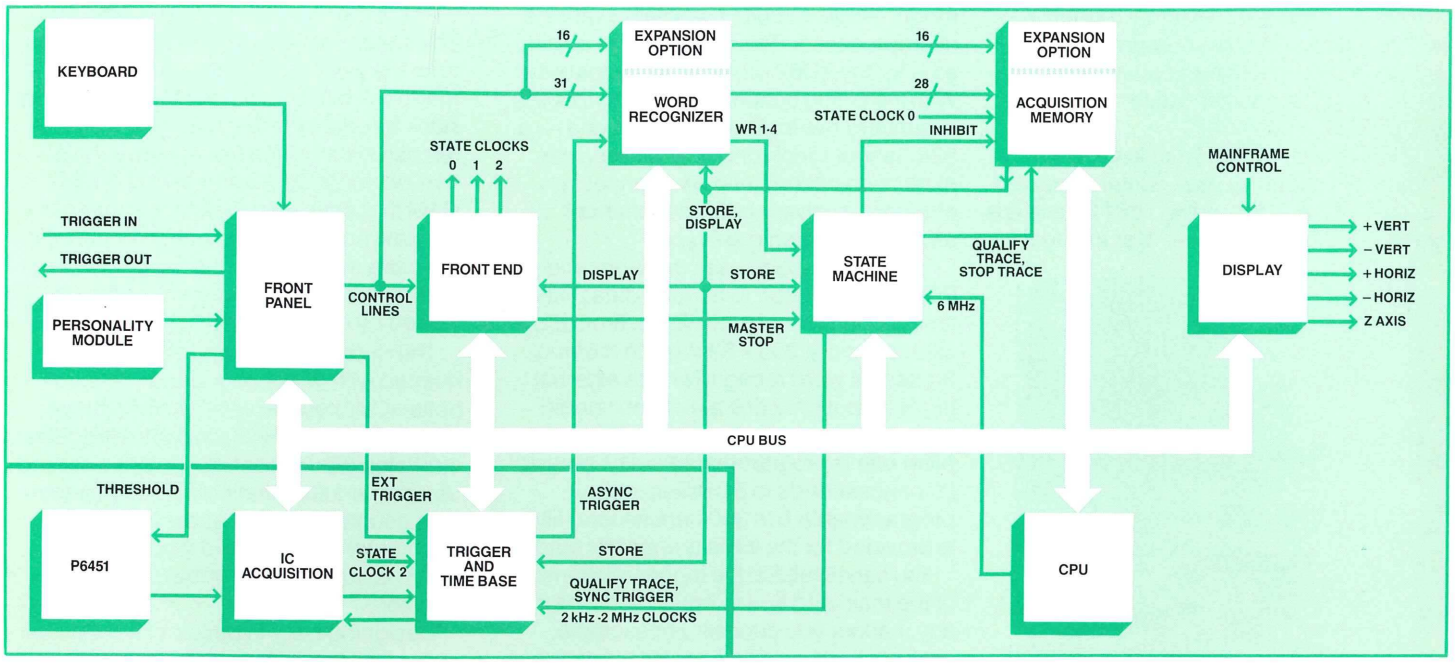


Fig. 5. Simplified block diagram of the 7D02 system. The expansion option allows the 7D02 to operate with 16-bit microprocessors and other systems, and extends the address lines to 24 and the data lines to 16. The timing option consists of the P6451, IC Acquisition, and Trigger and Time Base blocks.

to format the 7D02 input and output displays into the radices and mnemonics of the microprocessor under test.

To perform this format function, a special interpreter was developed. In display mode, data from the system is inhibited and the personality ROM is accessed via the acquisition bus. Commands are fetched from the personality module and executed by the interpreter. This approach allows extreme flexibility in designing future personality modules, saves coding space, and simplifies coding and debugging.

Self-test and diagnostic capabilities

An important consideration in using complex instrumentation is how to determine if it is working properly. The 7D02 has three levels of diagnostics to assist in this test.

At power-up, the 7D02 checks internal subsystems to the extent possible without having known data input. If problems exist, descriptive messages are displayed. These are keyed to troubleshooting trees in the 7D02 service manual.

The user can call up the Diagnostic Monitor — Module Test, which employs service test-generators contained in the personality modules. To verify all data paths through the system, the user plugs the acquisition probe into the service test socket, and the 7D02 acquires known input data and performs a checksum.

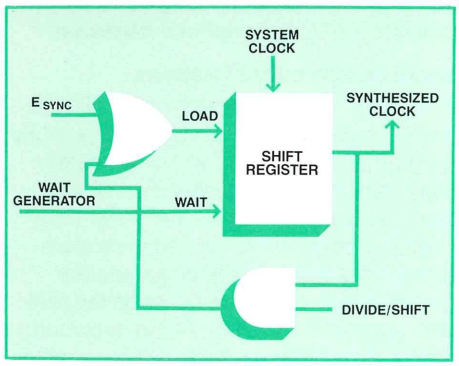


Fig. 6. Simplified block diagram of the 7D02's synthesized clock generator. Personality module firmware provides information to program the synthesizer and qualifier.

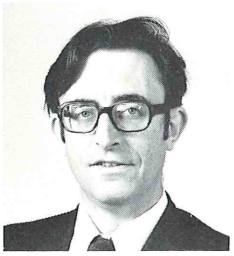
Suspect subsystems can be analyzed by using the Signature Exerciser Mode which generates test patterns that can be verified using a signature analyzer.

The diagnostic modes consume eight kilobytes of ROM (16% of the total firmware) and provide excellent diagnostic coverage of the 7D02 system.

Acknowledgements

Many people are involved in a project as extensive as the 7D02. While it isn't feasible to acknowledge each of them, I would like to express my thanks to all who worked so diligently on the project. Special thanks go to Dennis Glasby for the original 7D02 concept. Robin Teitzel was hardware project leader and Dave Moser performed a similar function for firmware. Paul Dittman, Steven Den Beste, Chris Benenati, and Bruce Ableidinger designed and implemented the firmware. The hardware team consisted of Vicky Tuite, Doug Boyce and Keith Taylor. Diagnostics are the work of Bob Heath, and the personality modules were the responsibility of Richard Jones. ■

Digital Storage and Plug-in Versatility Distinguish New 10-MHz 5000-Series Oscilloscope



Cliff Baker, project manager for the 5223, was educated in England and received his EE diploma from Oxford College of Technology. He has been involved with engineering 5000 Series products since coming to Tek six years ago. In his leisure time Cliff enjoys gardening and working with radio-controlled model airplanes.

Before the development of the storage oscilloscope, physical, mechanical, biomedical, and similar type measurements were difficult and time consuming to make. Direct-view-storage-tube oscilloscopes changed all of that. Now, a new storage instrument, the Tektronix 5223 Digitizer Oscilloscope, offers some exciting new capabilities.

In areas of biological research, such as stimulus-response and EMG studies, and in mechanical design applications, such as structural and engine-performance testing, the 5223 simplifies the data collection process. The 5223 takes the guesswork out of capturing single-shot waveforms by using two features — bislope triggering and pretrigger viewing. In addition to assured storage performance, the 5223 provides waveform retrieval via an X-Y output port to a chart recorder and waveform manipulation via the optional GPIB feature.

For display, the 5223 uses a high-resolution, 6½-inch cathode ray tube (CRT). Displayed waveforms are sharp and bright, and viewing time is unlimited. The large-screen CRT is ideal for viewing multitrace displays. As an example, the 5223 can display up to four stored signals simultaneously, and you can view real-time signals and stored signals together. Waveform measurements and comparisons are facilitated because you can reposition and expand the stored waveforms on-screen.

For signal acquisition, the 5223 uses the 5000-Series of vertical amplifier plug-ins. These offer wide-ranging capabilities from differential, 10-microvolt/division sensitivity, to gigahertz bandwidth using sampling techniques.

For real-time operation, any of the 5000-Series time bases can be used. The new 5B25N Digitizer Time Base plug-in provides digital storage operation. It includes features of special interest to users making physical, mechanical, biomedical, and similar type measurements. For example, when viewing single-occurrence events, the user often misses the information of interest because of the uncertainty with which the trigger signal is generated. This uncertainty is overcome with the 5B25N by using the bislope triggering mode (see figure 2). In this mode, either a positive or negative-going signal will trigger the sweep. The trigger level control serves as a sensitivity control to prevent premature triggering on noise or other extraneous signals.

One of the unique features of digital storage is the ability to capture events occurring prior to the trigger event. The 5B25N, with continuously variable pretrigger control, lets you position the trigger point anywhere on-screen. The pretrigger portion of the display is intensified for easy identification.

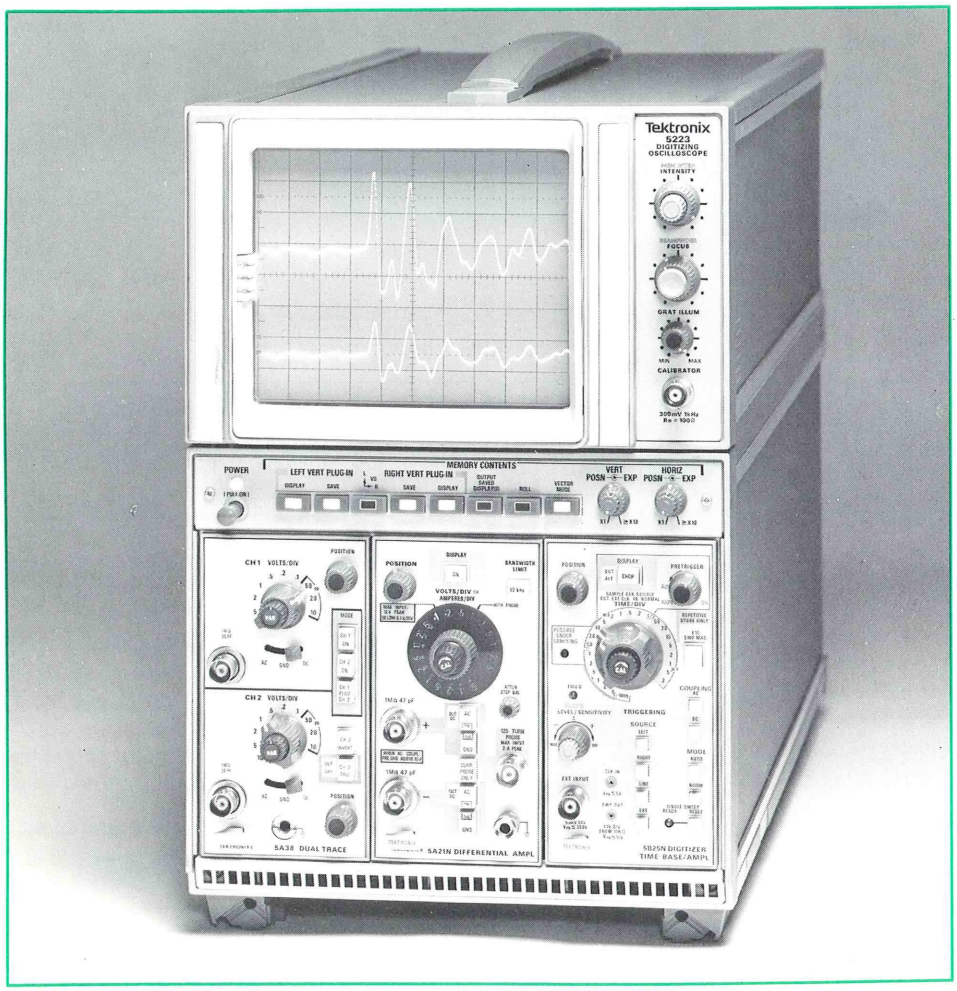


Fig. 1. The 5223 Digitizer Oscilloscope. With the 5B25N Time Base, the 5223 provides multitrace digital storage of repetitive events up to 10 MHz.

Display format selection

One of the most useful features of digital storage is the capability to display digitized data in several formats. For example, in some applications it is desirable to continuously monitor changes in variably-shaped signals without the interruptions of sweep retrace and holdoff time. The roll mode of the 5223 provides this capability. In this mode, the memory contents are continually updated and displayed, with new data moving from right to left on-screen

similar to a strip-chart recorder display (see figure 3). Should a point of particular interest appear on-screen, you can hold the display for further study by pressing the SAVE push button.

In many instances, it is helpful to display waveforms in other than the conventional Y-T format. With the waveforms in digital storage, you can elect to display them in an X-Y format. With two identical wide-bandwidth vertical amplifier plug-ins installed in the 5223, you can select the L VS R display mode and achieve 10-megahertz X-Y displays with less than five degrees of phase shift introduced by the instrument. When the real-time signal is displayed, you can view both the X-Y and Y-T information for a more comprehensive display.

The stored waveforms are available at rear-panel connectors for making hard copies on your analog X-Y plotter. A pen-lift signal and PLOTTER OUT speed adjustment are provided also.

Interpreting the display

Digital storage oscilloscopes usually display the digitized waveform as a series of dots. In some displays, perceptual aliasing (a type of optical illusion inherent in dot displays) occurs. The eye tends to visually connect adjacent points; however, the closest dots in screen position may not be the next in sequence. Perceptual aliasing is overcome in the 5223 by selecting the vector display mode. In this mode, the dots are connected by straight lines.

In addition to perceptual aliasing, dot displays can also show an "envelope error," which occurs when the dots do not fall on the peaks of the signal. The user may not be able to detect this condition even when using a vector display, as the actual signal could still be outside the waveform traced by the vectors. Switching to real-time operation quickly reveals if envelope error is occurring.

Another type of confusing display can occur when too few samples are taken to adequately reproduce the real-time signal. A POSSIBLE UNDERSAMPLING indicator on the 5B25N alerts the operator to this condition. The remedy is to choose a more appropriate TIME/DIV setting.

Digitizing the signal

The 5223 can capture repetitive events at speeds up to 10 megahertz, and single-occurrence events up to 100 kilohertz.

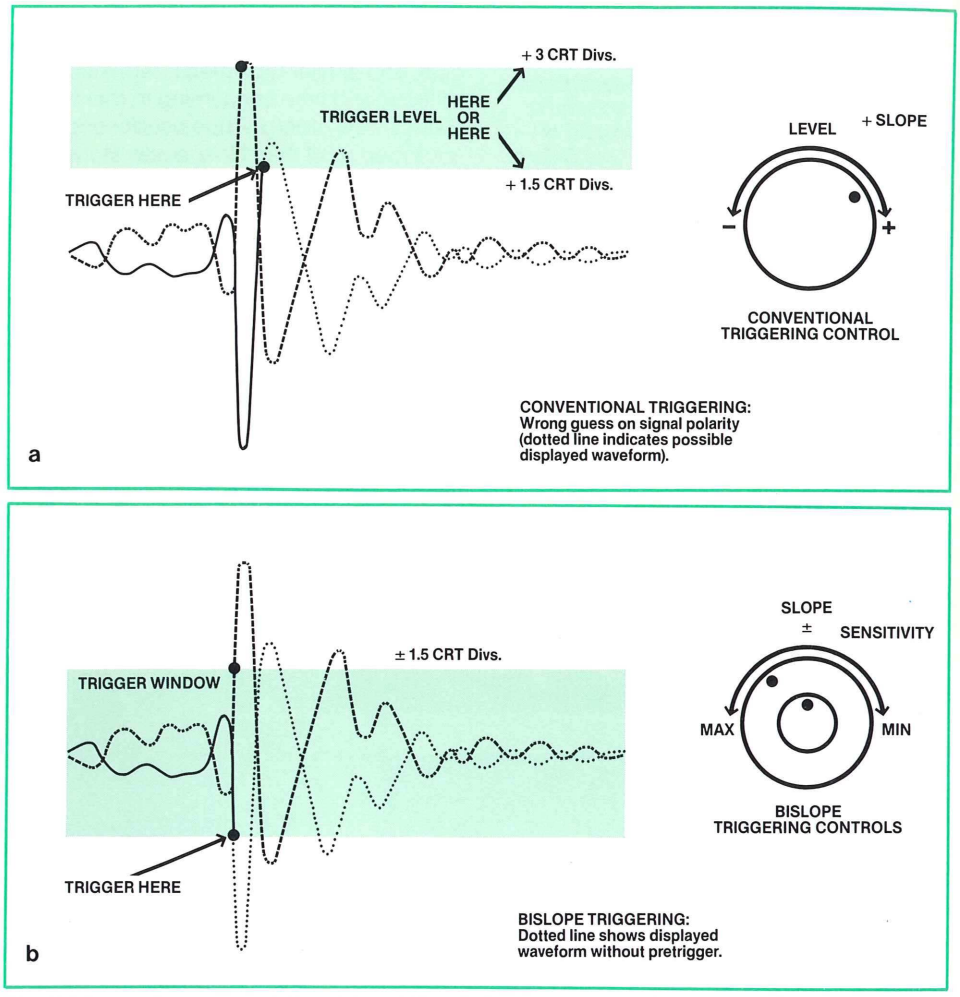


Fig. 2. Figure (a) at top shows how a conventional trigger circuit can miss a display if the signal originates with the opposite polarity than expected. If LEVEL had been set at +3 CRT divisions, sweep would never have been triggered. Figure (b) at bottom shows the operation of bislope triggering on the same waveform as depicted above.

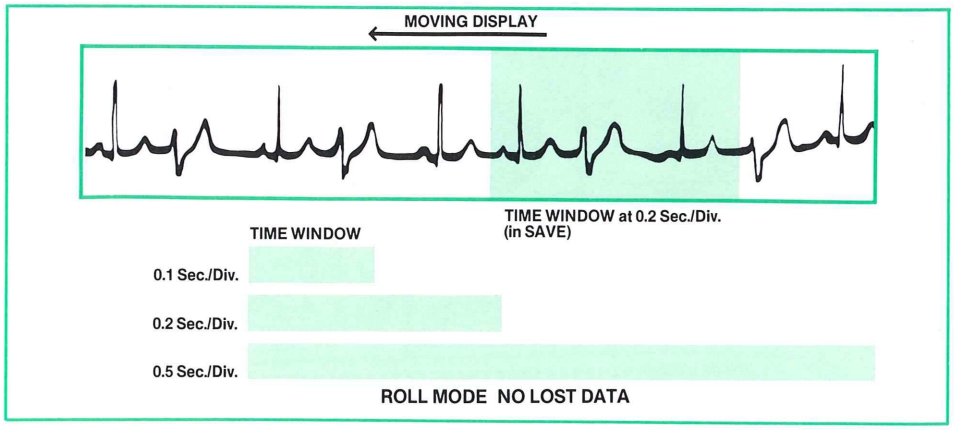


Fig. 3. The 5223's roll mode can capture signals without any loss of data due to sweep retrace/holdoff and triggering requirements. The time window is selected by the TIME/DIV control on the 5B25N Time Base.

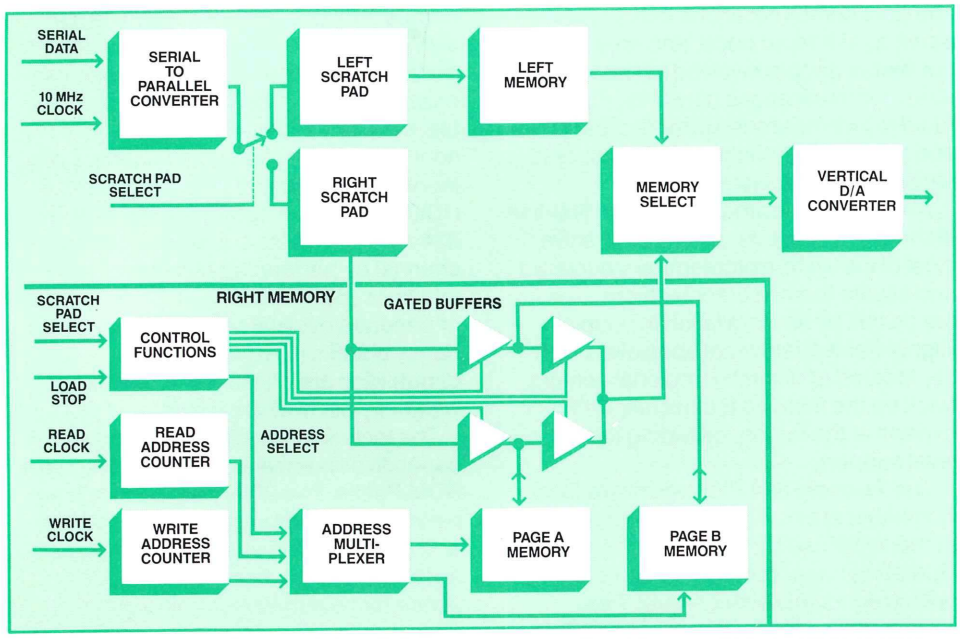


Fig. 4. Simplified block diagram of the 5223 memory system. The right memory is shown in detail to illustrate the two-page memory system that allows one page to be written while the other is being read, and vice versa. This scheme provides a flicker-free display.

Two types of sampling are used in the 5223. For sweep speeds of 0.1 milliseconds/division and slower, real-time sampling may be used. To store a complete waveform, 1024 samples are taken. The TIME/DIV control setting determines the sample rate. For sweep speeds of 50 microseconds division and faster, sequential-equivalent-time sampling is used, with one sample taken each sweep.

Both vertical channels of the 5223 are sampled simultaneously and then digitized sequentially. The analog-to-digital converter is a 10-bit successive approximation register that converts in one microsecond, allowing a maximum sampling rate of one megahertz.

The 1-megahertz clock from the digitizer enters serial data from the digitizer board into a serial-to-parallel converter. The 10-bit data bytes from the converter are temporarily stored in scratch-pad memories for later transfer to the left or right-compartment memory.

The memory system

The 5223 has two separate memory systems — one for each vertical compartment (see figure 4). Each memory system is, in turn, divided into two "pages" of 1024 words each. This arrangement allows the system to write data into one page, while reading data (for display purposes) from the other. Once a complete display cycle has occurred, the functions of the pages are interchanged (if the "acquisition" memory is fully loaded). This scheme ensures always having a full memory for display, and provides a flicker-free display. In the roll mode, page switching does not occur.

The memory output buffers are switched on, as appropriate, to apply the stored data to the vertical digital-to-analog converter. Conversion of the data from a full memory page takes about 4.5 milliseconds.

At sweep rates of 100 microseconds per division and slower, the display is chopped between the real-time signal and the stored signal. However, at faster sweep rates, the stored signal is displayed during the real-time sweep retrace, to reduce the likelihood of display flicker. This technique places some stringent requirements on the X and Y amplifiers as they have to switch to the "trace start" position and settle in less than the 0.25 microseconds provided by the delay line.

The optional GPIB

With the optional GPIB interface installed, the 5223's digital functions can be controlled via a controller such as the Tektronix 4052 Graphic Computing System. Because the 5223 is both a "talker" and a "listener," you can output waveforms for signal processing and data logging, or input externally recorded waveforms into the scope for comparison or reference purposes. Through software selection, the data can be output in binary or ASCII code.

Operating as a talker, the 5223 will output data continuously, a convenience for those applications requiring continuous data logging or real-time processing.

Summary

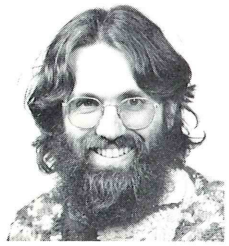
The 5223 combines digital storage, a real-time bandwidth of 10 megahertz, and plug-in versatility in an instrument designed to give you new measurement capability and operating ease. Multitrace storage, positioning and expansion of stored waveforms, X-Y plotter outputs, bislope triggering, pretrigger viewing, and other features provide important new measurement capability. The 5223 can be easily converted for rackmounting and occupies only seven inches of vertical rack space.

Acknowledgements

Many people are involved in the successful completion of a project like the 5223. My thanks to each one for their contribution. I would like to give special recognition to Mike Hurley for providing the original product definition; Gordon Meigs designed the memory system; Dave Dobak did the digitizer, power, and interface circuitry; the GPIB option is the work of Brian Rhodefer; and Roy Lewallen designed the 5B25N and X-Y circuitry.■

A Programmable Data Communications Tester for First-Line Technicians

Pete Janowitz was project leader for the 834 electrical engineering team. He started with Tek in 1968 and worked with portable scope engineering before joining the data communications analyzer group. Pete received his B.S.E.E. from Oregon State in 1964. He enjoys hiking, camping, and performing with a popular singing group.



John Light was software project leader for the 834 project. He has been involved in programming since 1968. John has two degrees from Cal State at L.A. —a B.S. in Mathematics ('70) and a B.A. in Psychology ('73). He joined Tek in 1977. John's off-work hours are spent in maintaining his small acreage on which he raises milk goats, and working with his personal computer.

The data communications industry is expanding at a rapid pace, and so is the number of people involved in servicing data communications networks. Such rapid growth has made it impractical to hire and train enough technical specialists to satisfy each user installation.

An alternate approach is to train first-line technicians to a level adequate to solve most of the system problems encountered, and situate them in branch offices. They are on call by an installation in trouble. Highly-trained technical specialists, usually located at district or regional centers, back up the first-line technician, with experts at the factory providing top level support.

The Tektronix 834 Programmable Data Communications Tester is designed primarily for use by first-line technicians. Operating ease, portability, and cost are optimized for this service level. Programmability and multifunction capability make the 834 a valuable tool for the technical specialist as well.

Multifunction capability

Now let's look at some of the 834's capabilities. The instrument can perform several functions. It can monitor data flow on both sides of the communications network, that is, data from the host computer or data from a remote terminal. The 834 also enables the user to simulate data terminal equipment (DTE) or data communications equipment (DCE). Extremely flexible, the 834 can be used with asynchronous or bisynchronous byte-oriented protocols, or bit-oriented protocols such as HDLC (high-level data-link control). The 834 can confirm the condition of the carrier channel by performing bit or block error rate tests (BERT/BLERT), and can display or generate cyclical or longitudinal redundancy checks (CRC/LRC). All of these capabilities are contained in a package weighing just twelve pounds.

The technician's ability to exercise these capabilities is enhanced through the use of ROM Packs. The ROM Packs provide an extended programming set and specific and general routines, stored messages, and test patterns. Each ROM Pack has space for customer-designed routines based on the customer's application. The first-line technician can, thus, use custom programs without needing to know the details of the programming language or taking the time to enter programs via the keyboard.

Microprocessor control provides versatility

Microprocessor control makes the 834 extremely versatile, yet easy to operate. It also simplifies the front-panel controls. The front-panel contains four major sections: a five-position mode switch, seven-button display control, 21-button keypad, and interface access panel.

A bright, 16-character, fluorescent display is used for parameter and message display, with the four right-hand characters forming a scratch pad area for data entry and character translation. Additionally, eight individual LEDs serve as indicators for control-line status and operational references.

The 834 provides a menu to assist the user in setting up the instrument for a particular function. For example, suppose we select the MONITOR mode. In this mode, the 834 passively looks at data on the channel and can acquire up to 2699 characters from the data stream. Captured data can then be displayed on the 16-character readout.

To check the operating parameters for the selected mode, we press the SETUP button. The first setup parameter displayed is display coding. This item in the menu

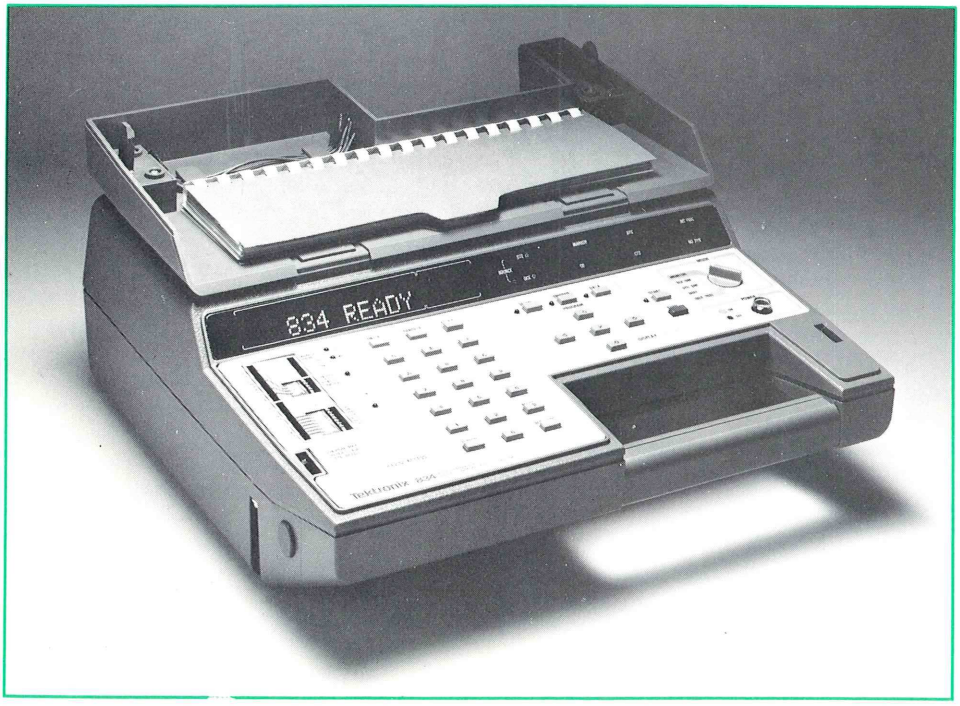


Fig. 1 The 834 Programmable Data Communications Tester.

allows us to select how the data will be formatted for display. The default mode is EBCDIC. Pressing the ← and → buttons will display the other codes available; in this instance, $EBCDIC_{Hx}$, ASCII, $ASCII_{Hx}$, and HEX. A user-defined code can also be used. In EBCDIC and ASCII, the control characters will be decoded as 3-character mnemonics in the scratch pad area. Should we want to operate on the control character via the keypad, it would be convenient to have the character displayed in HEX. By selecting $EBCDIC_{Hx}$ or $ASCII_{Hx}$, the control characters will be decoded as hexadecimal pairs in the scratch pad area. In the HEX mode, all characters are displayed as hexadecimal pairs.

To go to the next, or the previous, setup parameter, we use the ↑ or ↓ buttons. In our example, the next parameter to be setup is baud rate. We can choose from baud rates of 50 to 19,200 bits per second. Continuing on through the setup, we can select full or half-duplex operation, half-duplex turnaround, delay, synchronous, HDLC, or asynchronous operation, bits/characters, parity and so forth.

Triggering capability

A key element in the setup procedure is defining the trigger. The precision with which we can define the trigger point often determines whether we capture the data of interest. With the 834, we can choose: to capture data preceding, following, or centered around the trigger event; whether triggering will occur on DCE or DTE data, or neither; whether to trigger on an error condition; or whether to trigger on the positive or negative transition of one of the EIA control lines. We can program a 0-to-5 character sequence or use a mask to set up a 0-to-25 character sequence (see figure 3). The ability to mask select bits when comparing the trigger character to acquired data is useful in working with bit-oriented protocols, and enables the 834 to trigger on a particular address and control-bit combination. Trigger sequences are entered from the decimal keypad which is part of the 21-button keypad.

Pressing the START button begins data acquisition. If a trigger has been programmed, the NO TRIGGER light remains on until the trigger is found. When triggering occurs, data is captured relative to the trigger event as we have programmed it. During data acquisition, data characters are displayed as they are received.

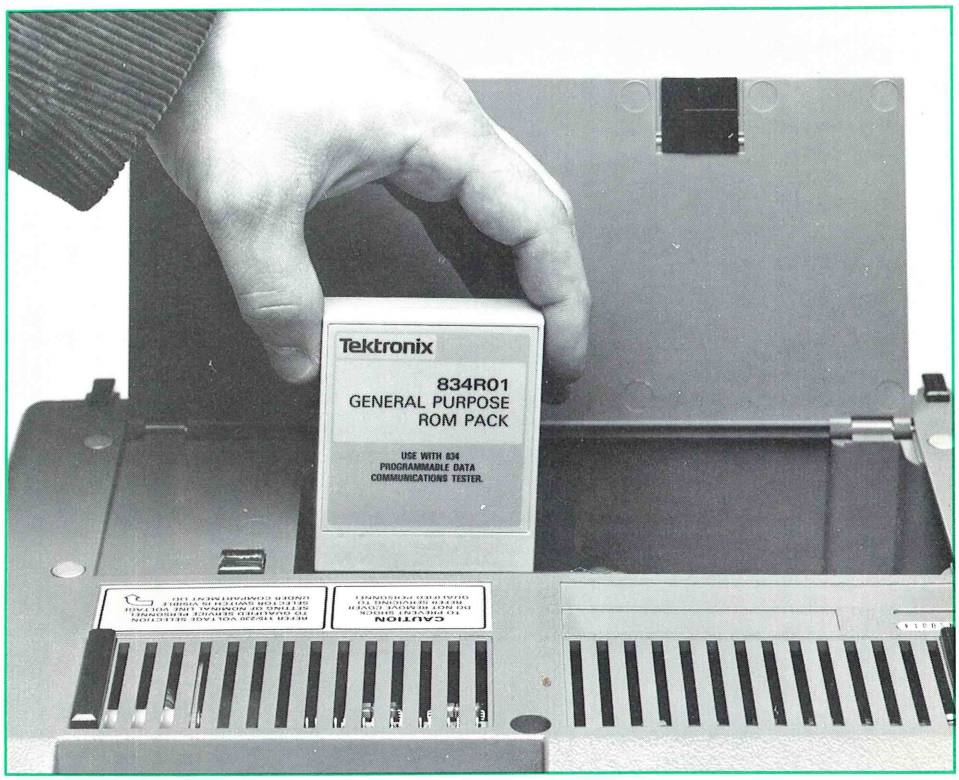


Fig. 2. Through the use of ROM Packs, the user can expand the capability of the 834 and employ programs customized for the system under test.

Source, error, and control line status also are displayed in real time.

After data acquisition, we can use the ← and → buttons to step through the capture-buffer contents. We can display any position in the buffer by entering (from the decimal keypad) the number of characters we want to shift and then pressing the ← or → button. The scratch pad area displays the hex equivalent of the right-most character in the display.

Normally, DTE and DCE characters are displayed in the order in which they are received. We can display only DCE or only DTE characters by pressing and holding the appropriate ↑ or ↓ button.

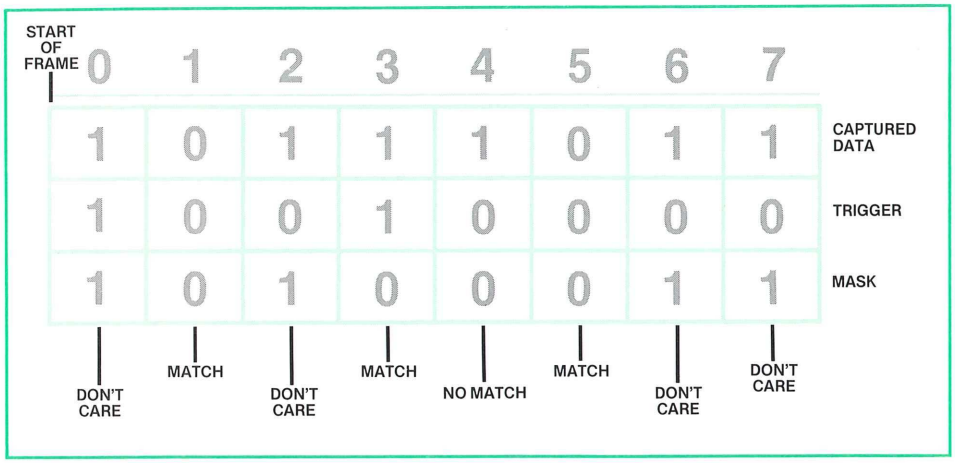


Fig. 3. A mask may be programmed to extend the 834's triggering capability. In this example, a match between data and trigger is attempted only where the mask contains a 0. There is no match, in this instance, because of the 1 in bit four.

Table 1. The basic 834 programming set includes 10 instructions. The ROM Packs provide a greatly extended set of instructions as shown here.

The programming instruction set resident in the basic 834 is as follows:

0 HALT:mm
Stop and display message MM

1 SEND:mm
Send contents of message buffer MM as a frame

2 RECEIVE
Obtain next complete data frame for processing

3 COMPARE:mm
Search frame for a match with message buffer MM

4 JUMP EQ→ss
Jump to step SS if a match is found

5 JUMP NE→ss
Jump to step SS if a match is not found

6 JUMP→ss
Jump to step SS

7 IF TIME→ss
Jump to step SS if the timer expires

8 TIMEOUT # pp
Start timer with value parameter PP

9 MASK:mm
Use message MM for mask during COMPARE operation

10 WAIT # pp
Start timer with value in parameter PP and do not proceed to following step until timer expires

A colon (:) indicates that the argument to be specified is a message.

A pound sign (#) indicates that the argument to be specified is a parameter.

An equal sign (=) indicates that the value to be specified is to be used in the execution of the instruction.

An arrow (→) indicates transfer to another program step.

The extended programming set contained in the ROM Packs consists of the following instructions:

11 LOAD # pp
Load register with value in parameter PP

12 STORE # pp
Store register value in parameter PP

13 COMPARE # pp
Compare register value to value in parameter PP

14 INCRMNT # pp
Increment value in parameter PP by one

15 DECRMNT # pp
Decrement value in parameter PP by one

16 DISPLAY # pp
Display value in parameter PP

17 LOAD:mm
Load register with character from message MM

18 STORE:mm
Store register value in message MM

19 DISPLAY:mm
Display message MM

20 CLEAR:mm
Clear message MM

21 TRANSFR # pp
Invoke key sequence described by value in parameter PP

22 SETEIA=nn
Set EIA RS-232 control line specified by value NN

23 TESTEIA=nn
Test EIA RS-232 control line specified by value NN

24 TESTFRM=nn
Test for type of frame indicated by value NN

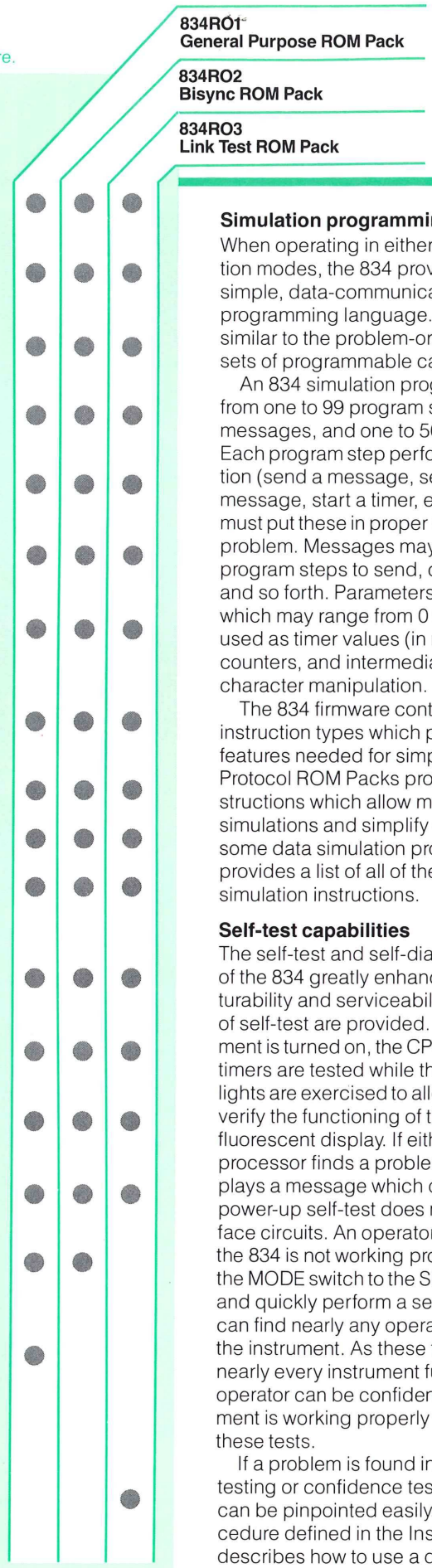
25 TESTKEY=nn
Test for keyboard input indicated by value NN

26 BREAK # pp
Send BREAK for length of time specified in parameter PP

27 BCC:mm
Calculate and insert BCC for message MM

28 NOP
Not available in present ROM Packs

29 BLOCK:mm
Compare frame to message buffer MM and count bit errors



Simulation programming

When operating in either of the two simulation modes, the 834 provides the user a simple, data-communications-oriented programming language. This language is similar to the problem-oriented instruction sets of programmable calculators.

An 834 simulation program consists of from one to 99 program steps, one to 50 messages, and one to 50 parameters. Each program step performs a single function (send a message, search a received message, start a timer, etc.). The users must put these in proper order to solve their problem. Messages may be invoked by program steps to send, compare, display, and so forth. Parameters are numbers which may range from 0 to 9999. They are used as timer values (in milliseconds), counters, and intermediate storage for character manipulation.

The 834 firmware contains eleven instruction types which provide most of the features needed for simple simulations. Protocol ROM Packs provide additional instructions which allow more complex simulations and simplify dealing with some data simulation protocols. Table 1 provides a list of all of the available simulation instructions.

Self-test capabilities

The self-test and self-diagnostics features of the 834 greatly enhance its manufacturability and serviceability. Several levels of self-test are provided. When the instrument is turned on, the CPU, ROM, RAM and timers are tested while the front-panel lights are exercised to allow the operator to verify the functioning of the LEDs and fluorescent display. If either microprocessor finds a problem, the 834 displays a message which describes it. The power-up self-test does not test the interface circuits. An operator, suspecting that the 834 is not working properly, may turn the MODE switch to the SELF TEST position and quickly perform a series of tests that can find nearly any operational problem in the instrument. As these tests exercise nearly every instrument function, the operator can be confident that the instrument is working properly if it passes these tests.

If a problem is found in either power-up testing or confidence testing, the problem can be pinpointed easily. The service procedure defined in the Instruction Manual describes how to use a digital voltmeter

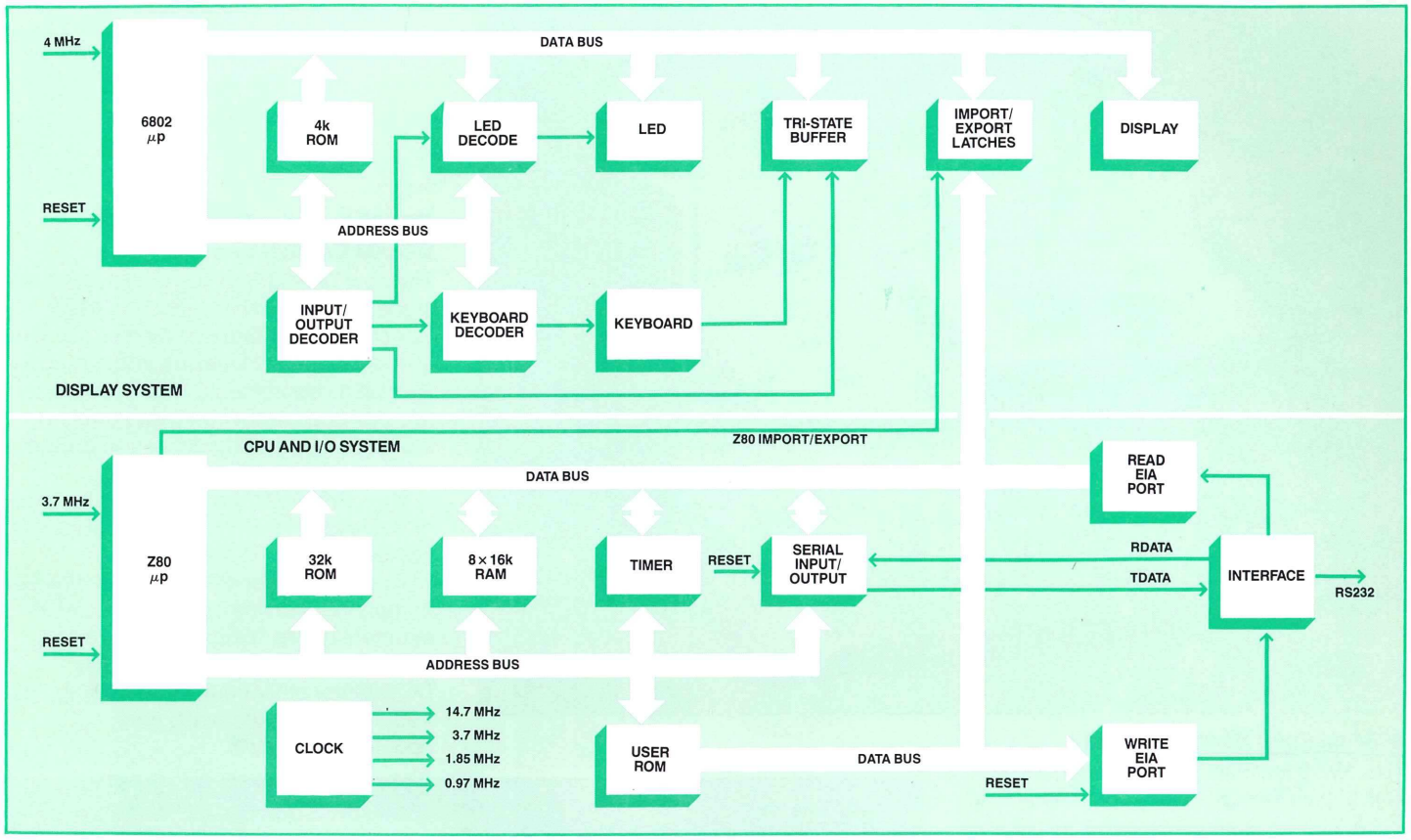


Fig. 4. Simplified block diagram of the 834. Separate microprocessors control the acquisition and display processes.

and frequency counter in conjunction with the Diagnostic ROM Pack to trace the problem to its source.

The system architecture

The 834 contains two microprocessor-controlled systems (see figure 4). A Z80 microprocessor runs the CPU and input/output system, while a 6802 (with self-contained RAM) handles the display processing.

The Z80 and 4 k of the 28 k bytes of ROM form the kernel of the CPU. The 4 k erasable ROM contains the initialization routines and power-up self-tests. Only power, a clock, and a reset pulse are needed for the kernel to function. If the kernel is functioning, the CPU can survey the rest of the 834 and identify system problems.

The 16 k bytes of RAM provide a space in which the CPU can store and retrieve data. Such data includes messages received from, or to be transmitted to, the RS-232 interface.

The serial input/output (SIO) chip plays a central role in the input/output function. It takes the 8-bit parallel data off the bus and then, under CPU control, serially transfers that data to the interface. Conversely, the SIO receives serial data from the interface and places it on the bus as parallel data.

The 834's internal timer is a programmable baud rate and interval generator which supplies transmit and receive clock signals. These signals are used in applications in which the 834 must provide its own clock or the system clock.

The interface does the signal conditioning between the RS-232 interface and the 834 I/O system. This includes shifting between RS-232 and TTL levels, decoding and encoding NRZI, selecting a timing source, and detecting transitions for the data-derived clock.

The display processor section of the 834 handles control and decoding for the keyboard, and for the LED and fluorescent displays. This section of the 834 is a complete microprocessor system containing its own 6802 microprocessor chip with on-board RAM, a 4-megahertz clock, 4 k ROM, LED drivers, and keyboard decoding.

Summary

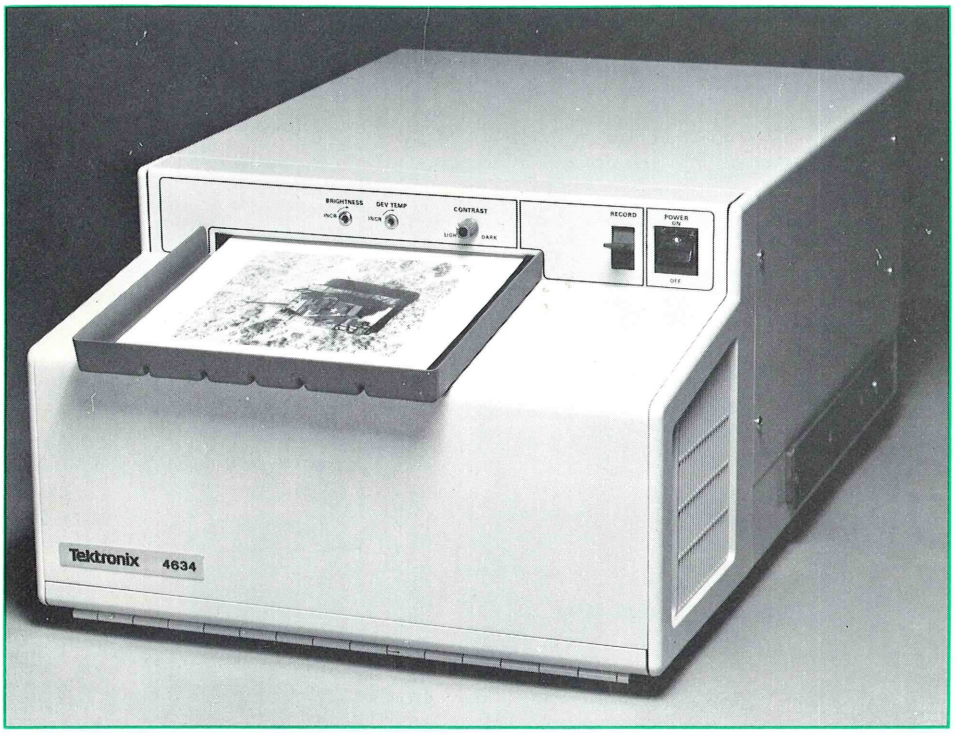
The 834 Programmable Data Communications Tester gives the user a wide range of capabilities in one compact, easy to use instrument. It is optimized for operation by the first-line technician. With the help of customized ROM Packs, the technician can perform sophisticated tests rapidly and accurately and should be able to solve most of the system problems encountered, on the first call.

Acknowledgements

We would like to express our appreciation to our cohorts in the hardware and software design teams for their individual contributions to the 834 project. Wendell Damm, project manager, provided overall direction and gave encouragement. Dave Thompson deserves special mention for his work on the service procedure, and Garth Eimers for his valuable marketing input.

New Products

High Resolution Hard Copier



4634 Imaging Hard Copy Unit

The Tektronix 4634 Imaging Hard Copy Unit produces high quality continuous tone copies from raster scan video sources in seconds. Designed to provide photographic quality images, the device is aimed primarily at digital image processing, pattern recognition, remote sensing, video disc and high resolution display environments.

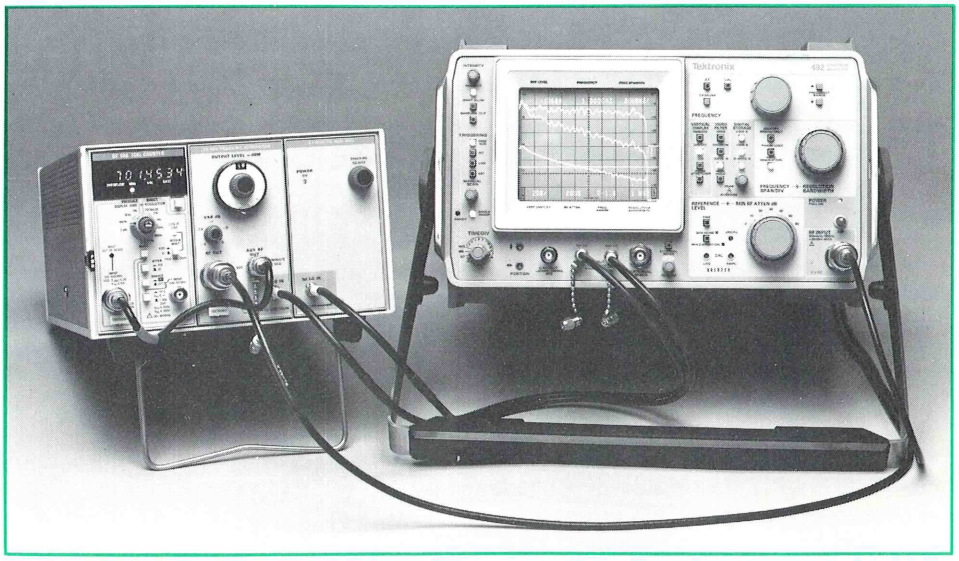
The 4634 records on dry silver paper using a fiber-optic CRT. Clean and convenient, the dry copy process requires no toners or developers. The high resolution copies have a broad gray scale range (12 levels) that reveals fine image detail, and the large 6 x 8-inch image size on 8½ x 11-inch paper makes details easy to see.

The cost per copy is substantially lower than that for similar competitive units.

Front paper load and exit, and front-panel controls make it easy to integrate the 4634 into video system configurations. It is self-contained, usually requiring a single cable connection, and can be interfaced to most raster scan video sources, either analog or digital.

An automatic gain control circuit tracks the input signal, making the 4634 less sensitive to input signal variations. Image quality is thus more consistent over time, with minimum adjustment required. ■

Tracking Generator for the 492-492P Spectrum Analyzers



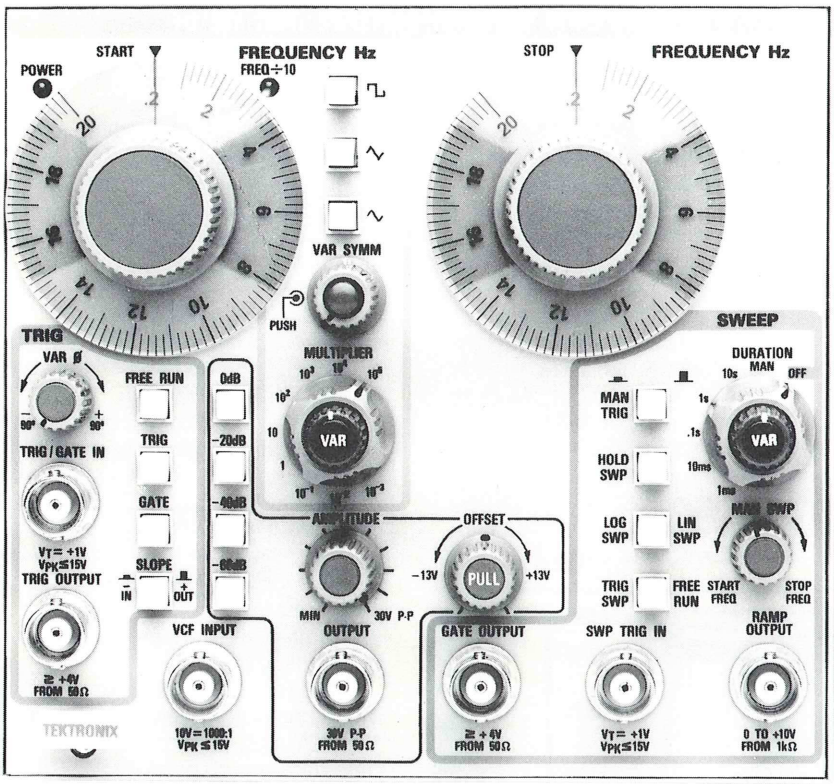
TR 503 Tracking Generator with DC 508 Counter and 492.

The new TR 503 Tracking Generator is designed to work with the 492 and 492P Spectrum Analyzers to provide state of the art performance in making frequency response measurements of passive and active devices, swept return loss measurements using an external passive bridge, and other applications.

The TR 503/492 has a frequency range of 100 kHz to 1.8 GHz with ±1.5 dB system flatness and 50 Hz stability.

The tracking generator is a two-wide unit compatible with the TM 500 Modular Instrument Series. When powered by a TM 503, there is room for a 1.3 GHz DC 508A or other counter for making frequency measurements with counter accuracy. ■

The New TM 500 Series Function Generators



FG 507 2-MHz Function Generator

Two new function generators broaden the signal generation capabilities of the versatile TM 500 Series instrumentation. The FG 501A provides low-distortion sine, square, triangle, ramp, and pulse waveforms from 0.002 Hz to 2 MHz in eight decade steps. Maximum output level is 30 V p-p into an open circuit, with up to ±13 V of dc offset from 50Ω. Waveform triggering, and gating are provided. A variable phase control permits phase shifts of up to ±90 degrees. Symmetry can be adjusted over a range of 5% to 95% to generate pulses and ramps. Pulse rise time is ≤25 ns. Push-button-selectable step attenuators provide 60 dB of attenuation in 20 dB steps, and a variable amplitude control provides an additional 20 dB of attenuation. A voltage-controlled-frequency input provides a 1000:1 ratio of swept frequency.

The FG 507 has all of the capabilities of the FG 501A, plus an internal sweep generator to internally sweep up to three decades of frequency with either a linear or logarithmic sweep. The log sweep allows accurate swept-frequency plots on log scales or paper. Separate start and stop frequency dials make swept-frequency measurements very easy. The FG 507 can sweep up or down in frequency, dependent on the setting of the two dials. A manual sweep capability is available also. The sweep can be free-run, or triggered either externally or manually. A sweep-hold mode allows the FG 507 to sweep to the stop frequency and remain there until released. ■

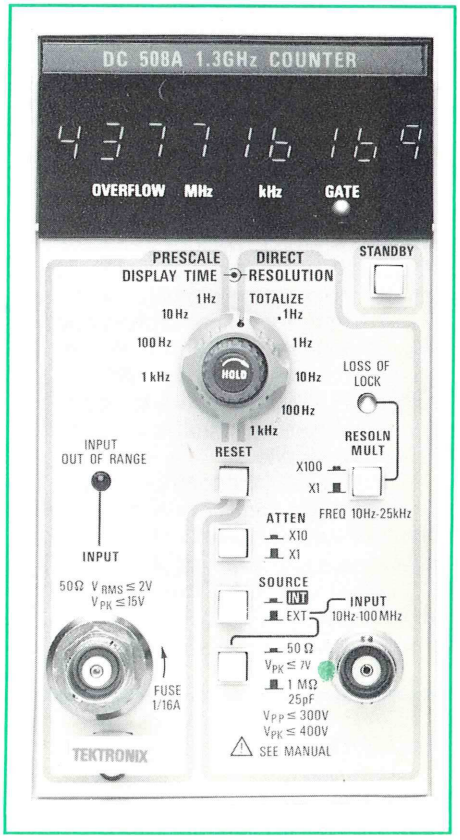
Counter Capability Extended to 1.3 GHz

DC 508A Frequency Counter

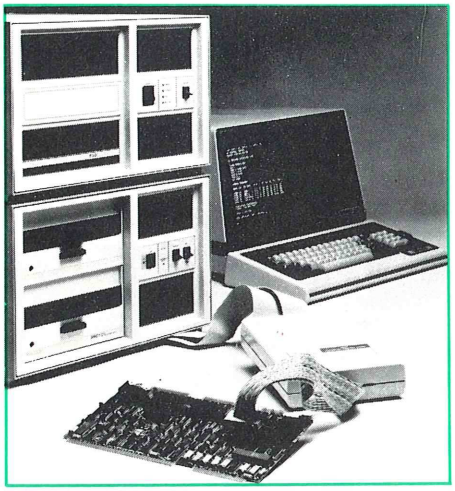
The DC 508A Counter, designed to operate in a TM 500 Series Power Module, measures frequency from 10 Hz to 1.3 GHz. The DC 508A provides a direct input for measuring frequencies from 10 Hz to 100 MHz and a prescaler input for frequencies from 100 MHz to 1.3 GHz. The DC 508A totalizes events from 0 to 999,999,999 over a frequency range of 10 Hz to 100 MHz.

A nine-digit display allows resolutions of 1 kHz to 1 Hz (0.1 Hz using direct input). An audio frequency resolution multiplier increases resolution by a factor of 100 times from 10 Hz to 25 kHz. This feature yields a resolution of 0.01 Hz in one second. Automatic decimal point positioning and blanking of leading zeros simplifies reading the display.

The direct input sensitivity is 15 mV RMS, and prescaler input sensitivity is 20 mV from 100 MHz to 1.1 GHz and 40 mV from 1.1 GHz to 1.3 GHz. The prescaler input has a VSWR of 2.2:1 or less and is protected by an easily-replaceable front-panel fuse. ■



A New Microprocessor Development Family



8550 Microcomputer Development Lab

The Tektronix 8550 Microcomputer Development Lab is the initial member of a new family of products (the 8500 Series) that will provide complete design, debugging, and integration tools for each of three major design environments: the single-user lab, multi-user lab, and host-computer operation.

The 8550 is a single-user lab and consists of two major components: the 8301 Microprocessor Development Unit and the 8501 Data Management Unit. The 8301 houses the operating system software, DOS/50, 32 kilobytes of static system memory, 32 kilobytes of static program memory, language processor, and emulator controller. Options include an additional 32 kilobytes of static program memory, the real-time prototype analyzer, and emulator processors. Optional systems software includes assemblers for all supported microprocessors, PASCAL and MDL/μ compilers for several supported microprocessors, and the Advanced CRT-oriented Editor.

The 8501 Data Management Unit handles files and auxiliary I/O for DOS/50 and manages the movement of user files between its dual-sided, double-density flexible discs and the Microprocessor Development Unit. Disc memory capacity is two megabytes.

The 8550 currently supports the following 8-bit chips: Intel 8085A, 8080A, 8048, 8049, 8041A, 8039, 8039-6, 8035, 8022, 8021; Motorola 6800, 6802, 6808; Fairchild F8; Mostek 3870, 3872, 3874, 3876; Zilog Z80A; Texas Instruments TMS9900, SBP9900; RCA 1802; and Rockwell 6500/A. Tektronix will soon offer full support, including emulation, for the Intel 8086/88, Zilog Z8001/2, the Motorola 68000 16-bit microcomputers, and the Motorola 6809 8-bit microcomputer.

The 8550 will be compatible with other members of the 8500 family. For example, the 8550 can be directly integrated into the 8560, which will be a complete microcomputer development system for up to eight work stations. Another member, the 8540 Advanced Integration Unit, will be a self-contained peripheral station that provides hardware/software integration in conjunction with a host computer. It also can be used to provide 16-bit emulation for a single-user system, like the existing 8002A.

New 128-pin LSI/VLSI/Hybrid Semiconductor Test System

S-3275 Semiconductor Test System

The introduction of the new S-3275 128-pin test system reaffirms Tektronix' commitment to provide test solutions in a changing and increasingly complex environment. It is consistent with our continuing support policy for our customer base.

The S-3275 features state of the art pattern generation and timing, and has an analog bandwidth unmatched in the industry. An expanded software system improves memory utilization, increases processing speed, and contains a networking option that permits the S-3275 to be interfaced to any large computer. The software enhancement is also downward compatible for all Tektronix S-3200 Series semiconductor test systems.

The S-3275 has 20-MHz functional capability and realtime error logging. The system's 128 data channels operate either as 64 input and 64 output channels, or as 64 input/output channels.

The pattern processor offers sophisticated pattern control and sequencing as well as algorithmic pattern generation. Four bits of pattern data (force, inhibit, compare, and mask) are sent by the processor to each pin electronics card at the 20-MHz rate. Force and compare pattern memories are 64 bits by 4k words deep; inhibit and mask pattern memories are 64 bits by 1k word deep.

In the algorithmic pattern generation mode, the pattern processor generates 12X, 12Y, 12Z, 16 force data, and 16 compare data bits on each cycle. The addresses can be scrambled by the topological memory (4k words by 12 bit), an integral part of the pattern processor.

The clock generator makes 16 clock phases available to the test station. Sixteen sets of timing data, including start, width, and cycle time can be programmed and selected on a cycle-by-cycle basis by the pattern processor, resulting in complex, split-cycle timing.

The networking option, an extension of the operating system software, provides the interface to user-defined mainframes. With the option, the user can interface the test system to any large computer to obtain central program management. ■

12/80 AX-4658

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077